WHAT IS CLAIMED IS:

1. A method of operating an integrated circuit having a memory array including at least one plane of memory cells, said memory cells comprising switch devices having a charge storage dielectric and which cells are arranged in a plurality of series-connected NAND strings, said method comprising the steps of:

biasing a channel region of a half-selected memory cell in an unselected NAND string of a selected memory block, to a first voltage; and then

capacitively coupling the channel region to a second voltage different than the first voltage when a selected word line associated with the half-selected memory cell transitions to a word line programming voltage, to thereby reduce a voltage potential between the selected word line and the channel region of the half-selected memory cell.

2. The method of claim 1 wherein the biasing step further comprises decoupling the half-selected memory cell from a bias source after establishing its channel region to the first voltage.

3. The method of claim 1 wherein the biasing step further comprises decoupling the half-selected memory cell from adjacent device channel regions after establishing the half-selected memory cell channel region to the first voltage.

4. The method as recited in claim 1 wherein the biasing step comprises:

(a) conveying a bit line inhibit voltage on a respective first array line associated with the unselected NAND string;

(b) coupling a first end of the unselected NAND string through a first group of at least one series selection device, to the respective first array line associated with the unselected NAND string; and

(c) turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string; and then

(d) decoupling the channel region of the half-selected memory cell from the respective first array line after establishing the half-selected memory cell channel region to the first voltage.

5. The method of claim 4 wherein step (c) comprises driving the word lines associated with the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the NAND string to a first passing voltage sufficient to turn on both programmed and unprogrammed memory cells to bias the half-selected memory cell channel to the first voltage.

6. The method of claim 5 wherein the first voltage is substantially equal to the bit line inhibit voltage.

7. The method of claim 5 wherein the first voltage is substantially less than the bit line inhibit voltage.

8. The method of claim 5 wherein step (c) further comprises driving all word lines associated with memory cells of the unselected NAND string to the first passing voltage.

9. The method of claim 4 wherein step (d) comprises turning off at least one memory cell adjacent to the half-selected memory cell.

10. The method of claim 4 wherein step (d) comprises turning off at least one device within the first group of at least one series selection device of the unselected NAND string.

11. The method of claim 4 wherein step (d) comprises driving the unselected word lines associated with the unselected NAND string to a second passing voltage different than the first passing voltage, said second passing voltage chosen such that both programmed and unprogrammed memory cells in the unselected NAND string are turned off, and such that voltage stress across unselected memory cells in a selected NAND string is reduced.

12. The method of claim 11 wherein word lines driven to the second passing voltage are driven directly from the first passing voltage to the second passing voltage.

13. The method of claim 11 wherein word lines driven to the second passing voltage are driven first from the first passing voltage to ground, and then driven to the second passing voltage.

14. The method of claim 4 further comprising:

(e) coupling a first end of a selected NAND string of the selected memory block through a first group of at least one series selection device, to a respective first array line associated with the selected NAND string, said respective first array line conveying a bit line programming voltage;

(f) coupling the bit line programming voltage to a channel region of a selected memory cell in the selected NAND string, said selected memory cell also associated with the selected word line;

15. The method of claim 14 further comprising:

(g) turning off at least one device of a second group of at least one series selection device at a second end of the unselected NAND string opposite the first end, said second group of at least one series selection device for coupling said unselected NAND string to a respective second array line associated with the unselected NAND string; and

(h) turning off at least one device of a second group of at least one series selection device at a second end of the selected NAND string opposite the first end, said second group of at least one series selection device for coupling said selected NAND string to a respective second array line associated with the unselected NAND string.

16. The method of claim 15 wherein:

the respective second group of at least one series selection device at the second end of the selected and unselected NAND strings each includes

at least two such selection devices, each device driven by one of a second group of select signals; and

the method further comprises driving at least two of the second group of select signals to different voltages chosen to reduce leakage current from the unselected NAND string to the respective second array line associated therewith, and to reduce leakage current from the selected NAND string to the respective second array line associated therewith, when the selected word line is driven to the word line programming voltage.

17. The method of claim 16 wherein:

the respective first array line for each NAND string comprises a respective global bit line associated therewith; and

the respective second array line for each NAND string comprises a shared bias node.

18. The method of claim 17 wherein:

the respective first group of at least one series selection device of each NAND string within the selected block numbers one such selection device; and

the respective second group of at least one series selection device of each NAND string within the selected block includes at least a first and second such selection devices.

19. The method of claim 18 wherein:

for the second group of at least one series selection device of each NAND string within the selected block, the select signal applied to the first selection device conveys a voltage that is less than the threshold voltage of the first selection device, relative to a voltage on the shared bias node, and the select signal applied to the second selection device conveys a voltage that is greater than the threshold voltage of the second selection device, relative to the shared bias node voltage.

20. The method of claim 16 wherein:

for the selected NAND string, the respective first array line comprises a respective global bit line associated therewith, and the respective second array line comprises a shared bias node; and

for the unselected NAND string, the respective first array line comprises a shared bias node associated therewith, and the respective second array line comprises a respective global bit line.

21. The method of claim 20 wherein:

the respective first group of at least one series selection device of each NAND string numbers at least two such selection devices; and

the respective second group of at least one series selection device of each NAND string numbers at least two such selection devices.

22. The method of claim 17 further comprising:

during at least a programming pulse on the selected word line, biasing the shared bias node to a voltage between the bit line inhibit voltage and the bit line programming voltage.

23. The method of claim 16 further comprising:

driving unselected word lines associated with memory cells between the selected memory cell and the second end of the selected NAND string to a third passing voltage closer to the programming voltage than is the second passing voltage at least during any selected word line programming pulse, to thereby reduce programming stress across such unselected memory cells.

24. The method of claim 23 further comprising:

applying multiple selected word line programming pulses, and re-establishing the voltage bias of the half-selected memory cell channel region before each such programming pulse.

25. The method of claim 24 wherein at least one of the multiple selected word line programming pulses is less than 20 microseconds in duration.

26. The method of claim 1 further comprising:

repeating the biasing and coupling steps for a given half-selected memory cell to provide a plurality of programming pulses and to re-establish a voltage bias of the half-selected memory cell channel region before each such programming pulse.

27. The method of claim 1 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

28. The method of claim 1 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

29. The method of claim 1 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

30. The method of claim 28 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

31. The method of claim 28 wherein the substrate comprises a polycrystalline substrate.

32. The method of claim 28 wherein the substrate comprises an insulating substrate.

33. The method of claim 28 wherein the switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

34. The method of claim 33 further comprising programming selected memory cells from a first depletion mode threshold voltage corresponding to an erased data state to a second depletion mode threshold voltage corresponding to a programmed data state.

35. The method of claim 33 further comprising periodic programming of the series selection devices to a higher threshold voltage than fabricated.

36. A method of operating an integrated circuit having a memory array including at least one plane of memory cells, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings, said method comprising the steps of:

biasing a channel region of a half-selected memory cell in an unselected NAND string of a selected memory block, to a first voltage; and then

capacitively coupling the channel region to a second voltage different than the first voltage when a selected word line associated with the half-selected memory cell transitions to a word line programming voltage, to thereby reduce a voltage potential between the selected word line and the channel region of the half-selected memory cell.

37. The method of claim 36 wherein the biasing step further comprises:

decoupling the half-selected memory cell from a bias source after establishing its channel region to the first voltage.

38. The method of claim 36 wherein the biasing step further comprises:

decoupling the half-selected memory cell from adjacent device channel regions after establishing the half-selected memory cell channel region to the first voltage.

39. The method as recited in claim 36 wherein the biasing step comprises:

(a) conveying a bit line inhibit voltage on a respective first array line associated with the unselected NAND string;

(b) coupling a first end of the unselected NAND string through a first group of at least one series selection device, to the respective first array line associated with the unselected NAND string; and

(c) turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string; and then

(d) decoupling the channel region of the half-selected memory cell from the respective first array line after establishing the half-selected memory cell channel region to the first voltage.

40. The method of claim 39 wherein step (c) comprises:
driving the word lines associated with the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the NAND string to a first passing voltage sufficient to turn on both programmed and unprogrammed memory cells to bias the half-selected memory cell channel to the first voltage.

41. The method of claim 40 wherein the first voltage is substantially equal to the bit line inhibit voltage.

42. The method of claim 40 wherein the first voltage is substantially less than the bit line inhibit voltage.

43. The method of claim 40 wherein step (c) further comprises:
driving all word lines associated with memory cells of the unselected NAND string to the first passing voltage.

44. The method of claim 39 wherein step (d) comprises:
turning off at least one memory cell adjacent to the half-selected memory cell.

45. The method of claim 39 wherein step (d) comprises:
turning off at least one device within the first group of at least one series selection device of the unselected NAND string.

46. The method of claim 39 wherein step (d) comprises:
driving the unselected word lines associated with the unselected NAND string to a second passing voltage different than the first passing voltage, said second passing voltage chosen such that both programmed and unprogrammed memory cells in the unselected NAND string are

turned off, and such that voltage stress across unselected memory cells in a selected NAND string is reduced.

47. The method of claim 46 wherein word lines driven to the second passing voltage are driven directly from the first passing voltage to the second passing voltage.

48. The method of claim 46 wherein word lines driven to the second passing voltage are driven first from the first passing voltage to ground, and then driven to the second passing voltage.

49. The method of claim 39 further comprising:

(e) coupling a first end of a selected NAND string of the selected memory block through a first group of at least one series selection device, to a respective first array line associated with the selected NAND string, said respective first array line conveying a bit line programming voltage;

(f) coupling the bit line programming voltage to a channel region of a selected memory cell in the selected NAND string, said selected memory cell also associated with the selected word line;

50. The method of claim 49 further comprising:

(g) turning off at least one device of a second group of at least one series selection device at a second end of the unselected NAND string opposite the first end, said second group of at least one series selection device for coupling said unselected NAND string to a respective second array line associated with the unselected NAND string; and

(h) turning off at least one device of a second group of at least one series selection device at a second end of the selected NAND string opposite the first end, said second group of at least one series selection device for coupling said selected NAND string to a respective second array line associated with the unselected NAND string.

51. The method of claim 50 wherein:

the respective second group of at least one series selection device at the second end of the selected and unselected NAND strings each includes at least two such selection devices, each device driven by one of a second group of select signals; and

the method further comprises driving at least two of the second group of select signals to different voltages chosen to reduce leakage current from the unselected NAND string to the respective second array line associated therewith, and to reduce leakage current from the selected NAND string to the respective second array line associated therewith, when the selected word line is driven to the word line programming voltage.

52. The method of claim 51 wherein:

the respective first array line for each NAND string comprises a respective global bit line associated therewith; and

the respective second array line for each NAND string comprises a shared bias node.

53. The method of claim 52 wherein:

the respective first group of at least one series selection device of each NAND string within the selected block numbers one such selection device; and

the respective second group of at least one series selection device of each NAND string within the selected block includes at least a first and second such selection devices.

54. The method of claim 53 wherein:

for the second group of at least one series selection device of each NAND string within the selected block, the select signal applied to the first selection device conveys a voltage that is less than the threshold voltage of the first selection device, relative to a voltage on the shared bias node, and the select signal applied to the second selection device conveys a voltage that is greater than the threshold voltage of the second selection device, relative to the shared bias node voltage.

55. The method of claim 51 wherein:

for the selected NAND string, the respective first array line comprises a respective global bit line associated therewith, and the respective second array line comprises a shared bias node; and

for the unselected NAND string, the respective first array line comprises a shared bias node associated therewith, and the respective second array line comprises a respective global bit line.

56. The method of claim 55 wherein:

the respective first group of at least one series selection device of each NAND string numbers at least two such selection devices; and

the respective second group of at least one series selection device of each NAND string numbers at least two such selection devices.

57. The method of claim 52 further comprising:

during at least a programming pulse on the selected word line, biasing the shared bias node to a voltage between the bit line inhibit voltage and the bit line programming voltage.

58. The method of claim 51 further comprising:

driving unselected word lines associated with memory cells between the selected memory cell and the second end of the selected NAND string to a third passing voltage closer to the programming voltage than is the second passing voltage at least during any selected word line programming pulse, to thereby reduce programming stress across such unselected memory cells.

59. The method of claim 58 further comprising:

applying multiple selected word line programming pulses, and re-establishing the voltage bias of the half-selected memory cell channel region before each such programming pulse.

60. The method of claim 59 wherein at least one of the multiple selected word line programming pulses is less than 20 microseconds in duration.

61. The method of claim 36 further comprising:

repeating the biasing and coupling steps for a given half-selected memory cell to provide a plurality of programming pulses and to re-establish a voltage bias of the half-selected memory cell channel region before each such programming pulse.

62. The method of claim 36 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

63. The method of claim 62 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

64. The method of claim 62 wherein the substrate comprises a polycrystalline substrate.

65. The method of claim 62 wherein the substrate comprises an insulating substrate.

66. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise transistors having a charge storage dielectric.

67. The method of claim 66 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

68. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise a floating gate electrode.

69. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

70. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

71. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

72. The method of claim 36 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

73. The method of claim 72 further comprising programming selected memory cells from a first depletion mode threshold voltage corresponding to an erased data state to a second depletion mode threshold voltage corresponding to a programmed data state.

74. The method of claim 72 further comprising periodic programming of the series selection devices to a higher threshold voltage than fabricated.

75. An integrated circuit comprising:

a memory array having at least one plane of memory cells, said memory cells comprising switch devices having a charge storage dielectric and which cells are arranged in a plurality of series-connected NAND strings; and

means for biasing a channel region of a half-selected memory cell in an unselected NAND string of a selected memory block, to a first voltage; and

means for capacitively coupling the channel region to a second voltage different than the first voltage when a selected word line associated with the half-selected memory cell transitions to a word line programming voltage, to thereby reduce a voltage potential between the selected word line and the channel region of the half-selected memory cell.

76. The integrated circuit of claim 75 wherein the half-selected memory cell is decoupled from a bias source after establishing its channel region to the first voltage.

77. The integrated circuit of claim 75 wherein the half-selected memory cell is decoupled from adjacent device channel regions after establishing the half-selected memory cell channel region to the first voltage.

78. The integrated circuit of claim 75 wherein the means for biasing comprises:

means for conveying a bit line inhibit voltage on a respective first array line associated with the unselected NAND string;

means for coupling a first end of the unselected NAND string through a first group of at least one series selection device, to the respective first array line associated with the unselected NAND string; and

means for turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string; and

means for decoupling the channel region of the half-selected memory cell from the respective first array line after establishing the half-selected memory cell channel region to the first voltage.

79. The integrated circuit of claim 78 wherein the means for means for turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string includes:

means for driving the word lines associated with the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the NAND string are driven to a first passing voltage sufficient to turn on both programmed and unprogrammed memory cells to bias the half-selected memory cell channel to the first voltage.

80. The integrated circuit of claim 79 wherein the first voltage is substantially equal to the bit line inhibit voltage.

81. The integrated circuit of claim 79 wherein the first voltage is substantially less than the bit line inhibit voltage.

82. The integrated circuit of claim 79 wherein the means for means for turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string further includes:

means for driving all word lines associated with memory cells of the unselected NAND string to the first passing voltage.

83. The integrated circuit of claim 78 wherein the means for decoupling comprises:

means for turning off at least one memory cell adjacent to the half-selected memory cell.

84. The integrated circuit of claim 78 wherein the means for decoupling comprises:

means for turning off at least one device within the first group of at least one series selection device of the unselected NAND string.

85. The integrated circuit of claim 78 wherein the means for decoupling comprises:

means for driving the unselected word lines associated with the unselected NAND string to a second passing voltage different than the first passing voltage, said second passing voltage chosen such that both programmed and unprogrammed memory cells in the unselected NAND string are turned off, and such that voltage stress across unselected memory cells in a selected NAND string is reduced.

86. The integrated circuit of claim 85 wherein word lines driven to the second passing voltage are driven directly from the first passing voltage to the second passing voltage.

87. The integrated circuit of claim 85 wherein word lines driven to the second passing voltage are driven first from the first passing voltage to ground, and then driven to the second passing voltage.

88. The integrated circuit of claim 78 further comprising:

means for coupling a first end of a selected NAND string of the selected memory block through a first group of at least one series selection device, to a respective first array line associated with the selected NAND string, said respective first array line conveying a bit line programming voltage;

means for coupling the bit line programming voltage to a channel region of a selected memory cell in the selected NAND string, said selected memory cell also associated with the selected word line;

89. The integrated circuit of claim 88 further comprising:

means for turning off at least one device of a second group of at least one series selection device at a second end of the unselected NAND string opposite the first end, said second group of at least one series selection device for coupling said unselected NAND string to a respective second array line associated with the unselected NAND string; and

means for turning off at least one device of a second group of at least one series selection device at a second end of the selected NAND string opposite the first end, said second group of at least one series selection device for coupling said selected NAND string to a respective second array line associated with the unselected NAND string.

90. The integrated circuit of claim 89 wherein:

the respective second group of at least one series selection device at the second end of the selected and unselected NAND strings each includes at least two such selection devices, each device driven by one of a second group of select signals; and

at least two of the second group of select signals are driven to different voltages chosen to reduce leakage current from the unselected NAND

string to the respective second array line associated therewith, and to reduce leakage current from the selected NAND string to the respective second array line associated therewith, when the selected word line is driven to the word line programming voltage.

91. The integrated circuit of claim 90 wherein:

the respective first array line for each NAND string comprises a respective global bit line associated therewith; and

the respective second array line for each NAND string comprises a shared bias node.

92. The integrated circuit of claim 91 wherein:

the respective first group of at least one series selection device of each NAND string within the selected block numbers one such selection device; and

the respective second group of at least one series selection device of each NAND string within the selected block includes at least a first and second such selection devices.

93. The integrated circuit of claim 92 wherein:

for the second group of at least one series selection device of each NAND string within the selected block, the select signal applied to the first selection device conveys a voltage that is less than the threshold voltage of the first selection device, relative to a voltage on the shared bias node, and the select signal applied to the second selection device conveys a voltage that is greater than the threshold voltage of the second selection device, relative to the shared bias node voltage.

94. The integrated circuit of claim 90 wherein:

for the selected NAND string, the respective first array line comprises a respective global bit line associated therewith, and the respective second array line comprises a shared bias node; and

for the unselected NAND string, the respective first array line comprises a shared bias node associated therewith, and the respective second array line comprises a respective global bit line.

95. The integrated circuit of claim 94 wherein:
the respective first group of at least one series selection device of each NAND string numbers at least two such selection devices; and
the respective second group of at least one series selection device of each NAND string numbers at least two such selection devices.

96. The integrated circuit of claim 91 wherein:
during at least a programming pulse on the selected word line, the shared bias node is driven to a voltage between the bit line inhibit voltage and the bit line programming voltage.

97. The integrated circuit of claim 90 wherein:
unselected word lines associated with memory cells between the selected memory cell and the second end of the selected NAND string are driven to a third passing voltage closer to the programming voltage than is the second passing voltage at least during any selected word line programming pulse, to thereby reduce programming stress across such unselected memory cells.

98. The integrated circuit of claim 97 configured to apply multiple selected word line programming pulses, and to re-establish the voltage bias of the half-selected memory cell channel region before each such programming pulse.

99. The integrated circuit of claim 98 wherein at least one of the multiple selected word line programming pulses is less than 20 microseconds in duration.

100. The integrated circuit of claim 75 configured to apply multiple selected word line programming pulses, and to re-establish the voltage bias of the half-selected memory cell channel region before each such programming pulse.

101. The integrated circuit of claim 75 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

102. The integrated circuit of claim 75 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

103. The integrated circuit of claim 75 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

104. The integrated circuit of claim 102 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

105. The integrated circuit of claim 102 wherein the substrate comprises a polycrystalline substrate.

106. The integrated circuit of claim 102 wherein the substrate comprises an insulating substrate.

107. The integrated circuit of claim 102 wherein the switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

108. The integrated circuit of claim 107 the memory cell transistors have a first depletion mode threshold voltage corresponding to an erased data state and have a second depletion mode threshold voltage corresponding to a programmed data state.

109. The integrated circuit of claim 75 wherein the memory cell switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

110. The integrated circuit of claim 75 wherein the memory cell devices and series selection devices forming each NAND string are structurally substantially identical.

111. The integrated circuit of claim 75 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.

112. An integrated circuit comprising:

a memory array having at least one plane of memory cells, said memory cells comprising thin film modifiable conductance switch devices and which cells are arranged in a plurality of series-connected NAND strings; and

means for biasing a channel region of a half-selected memory cell in an unselected NAND string of a selected memory block, to a first voltage; and

means for capacitively coupling the channel region to a second voltage different than the first voltage when a selected word line associated with the half-selected memory cell transitions to a word line programming voltage, to thereby reduce a voltage potential between the selected word line and the channel region of the half-selected memory cell.

113. The integrated circuit of claim 112 wherein the half-selected memory cell is decoupled from a bias source after establishing its channel region to the first voltage.

114. The integrated circuit of claim 112 wherein the half-selected memory cell is decoupled from adjacent device channel regions after establishing the half-selected memory cell channel region to the first voltage.

115. The integrated circuit as recited in claim 112 wherein the means for biasing comprises:

means for conveying a bit line inhibit voltage on a respective first array line associated with the unselected NAND string;

means for coupling a first end of the unselected NAND string through a first group of at least one series selection device, to the respective first array line associated with the unselected NAND string; and

means for turning on the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the unselected NAND string; and

means for decoupling the channel region of the half-selected memory cell from the respective first array line after establishing the half-selected memory cell channel region to the first voltage.

116. The integrated circuit of claim 115 wherein the turning on means is configured for driving the word lines associated with the half-selected memory cell and any intervening memory cells between the half-selected memory cell and the first end of the NAND string to a first passing voltage sufficient to turn on both programmed and unprogrammed memory cells to bias the half-selected memory cell channel to the first voltage.

117. The integrated circuit of claim 116 wherein the first voltage is substantially equal to the bit line inhibit voltage.

118. The integrated circuit of claim 116 wherein the first voltage is substantially less than the bit line inhibit voltage.

119. The integrated circuit of claim 116 wherein the turning on means is configured for driving all word lines associated with memory cells of the unselected NAND string to the first passing voltage.

120. The integrated circuit of claim 115 wherein the decoupling means is configured for turning off at least one memory cell adjacent to the half-selected memory cell.

121. The integrated circuit of claim 115 wherein the decoupling means is configured for turning off at least one device within the first group of at least one series selection device of the unselected NAND string.

122. The integrated circuit of claim 115 wherein the decoupling means is configured for driving the unselected word lines associated with the unselected NAND string to a second passing voltage different than the first passing voltage, said second passing voltage chosen such that both programmed and unprogrammed memory cells in the unselected NAND string are turned off, and such that voltage stress across unselected memory cells in a selected NAND string is reduced.

123. The integrated circuit of claim 122 wherein word lines driven to the second passing voltage are driven directly from the first passing voltage to the second passing voltage.

124. The integrated circuit of claim 122 wherein word lines driven to the second passing voltage are driven first from the first passing voltage to ground, and then driven to the second passing voltage.

125. The integrated circuit of claim 115 further comprising:

means for coupling a first end of a selected NAND string of the selected memory block through a first group of at least one series selection device, to a respective first array line associated with the selected NAND string, said respective first array line conveying a bit line programming voltage;

means for coupling the bit line programming voltage to a channel region of a selected memory cell in the selected NAND string, said selected memory cell also associated with the selected word line;

126. The integrated circuit of claim 125 further comprising:

means for turning off at least one device of a second group of at least one series selection device at a second end of the unselected NAND string opposite the first end, said second group of at least one series selection device for coupling said unselected NAND string to a respective second array line associated with the unselected NAND string; and

means for turning off at least one device of a second group of at least one series selection device at a second end of the selected NAND string

opposite the first end, said second group of at least one series selection device for coupling said selected NAND string to a respective second array line associated with the unselected NAND string.

127. The integrated circuit of claim 126 wherein:

the respective second group of at least one series selection device at the second end of the selected and unselected NAND strings each includes at least two such selection devices, each device driven by one of a second group of select signals; and

at least two of the second group of select signals are driven to different voltages chosen to reduce leakage current from the unselected NAND string to the respective second array line associated therewith, and to reduce leakage current from the selected NAND string to the respective second array line associated therewith, when the selected word line is driven to the word line programming voltage.

128. The integrated circuit of claim 127 wherein:

the respective first array line for each NAND string comprises a respective global bit line associated therewith; and

the respective second array line for each NAND string comprises a shared bias node.

129. The integrated circuit of claim 128 wherein:

the respective first group of at least one series selection device of each NAND string within the selected block numbers one such selection device; and

the respective second group of at least one series selection device of each NAND string within the selected block includes at least a first and second such selection devices.

130. The integrated circuit of claim 129 wherein:

for the second group of at least one series selection device of each NAND string within the selected block, the select signal applied to the first selection device conveys a voltage that is less than the threshold

voltage of the first selection device, relative to a voltage on the shared bias node, and the select signal applied to the second selection device conveys a voltage that is greater than the threshold voltage of the second selection device, relative to the shared bias node voltage.

131. The integrated circuit of claim 127 wherein:

for the selected NAND string, the respective first array line comprises a respective global bit line associated therewith, and the respective second array line comprises a shared bias node; and

for the unselected NAND string, the respective first array line comprises a shared bias node associated therewith, and the respective second array line comprises a respective global bit line.

132. The integrated circuit of claim 131 wherein:

the respective first group of at least one series selection device of each NAND string numbers at least two such selection devices; and

the respective second group of at least one series selection device of each NAND string numbers at least two such selection devices.

133. The integrated circuit of claim 128 wherein:

during at least a programming pulse on the selected word line, the shared bias node is biased to a voltage between the bit line inhibit voltage and the bit line programming voltage.

134. The integrated circuit of claim 127 wherein:

unselected word lines associated with memory cells between the selected memory cell and the second end of the selected NAND string are driven to a third passing voltage closer to the programming voltage than is the second passing voltage at least during any selected word line programming pulse, to thereby reduce programming stress across such unselected memory cells..

135. The integrated circuit of claim 134 configured to:

apply multiple selected word line programming pulses, and re-establish the voltage bias of the half-selected memory cell channel region before each such programming pulse.

136. The integrated circuit of claim 135 wherein at least one of the multiple selected word line programming pulses is less than 20 microseconds in duration.

137. The integrated circuit of claim 112 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

138. The integrated circuit of claim 137 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

139. The integrated circuit of claim 137 wherein the substrate comprises a polycrystalline substrate.

140. The integrated circuit of claim 137 wherein the substrate comprises an insulating substrate.

141. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise transistors having a charge storage dielectric.

142. The integrated circuit of claim 141 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

143. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise a floating gate electrode.

144. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise silicon nanoparticles.

145. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise a polarizable material.

146. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise a ferroelectric material.

147. The integrated circuit of claim 112 wherein the thin film modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage for at least one of two data states.

148. The integrated circuit of claim 147 the memory cell transistors have a first depletion mode threshold voltage corresponding to an erased data state and have a second depletion mode threshold voltage corresponding to a programmed data state.

149. The integrated circuit of claim 112 wherein the memory cell switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

150. The integrated circuit of claim 112 wherein the memory cell devices and series selection devices forming each NAND string are structurally substantially identical.

151. The integrated circuit of claim 112 embodied in computer readable descriptive form suitable for design, test, or fabrication of the integrated circuit.